Highly Integrated Three-Dimensional MMIC Single-Chip Receiver and Transmitter

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***Abstract*—The three-dimensional monolithic microwave/millimeter wave integrated circuits (MMIC) structure that places thin polyimide-film layers on wafers significantly increases the integration level of MMIC's. We newly develop 9.2–12 GHz receiver and 9.5–14 GHz transmitter chips with 20 dB gain using the three-dimensional MMIC technology. The receiver chip includes a four-stage front-end amplifier, a local oscillator (LO) amplifier, and an image-rejecton mixer in a 2 × 2 mm chip. The transmitter chip also includes an IF amplifier with balanced outputs, an LO amplifier, an RF buffer amplifier, and a balanced upconverter in a 1.9 × 1.9 mm chip. The integration levels of these chips are nearly three times higher than those of conventional planar devices. The design method of each function block, such as the amplifier and mixer, is also described.**

I. Introduction

THE SPREAD of commercial wireless communication systems has resulted in increasing demand for highly integrated multifunctional monolithic microwave/millimeter wave integrated circuits (MMIC). Recently, many single-chip MMIC approaches in planar forms for miniaturizing receivers and transmitters have been reported [1]. However, the integration level I, defined as gain (G in dB)-bandwidth ($\Delta f/f_0$) product per mm^2, follows the curve $I \times [f(\mathrm{GHz})]^{1/2} = 2$ ($I = 0.6$ at 10 GHz) because of the very limited bandwidth and conversion gain obtained from the small area [1], [2]. We have developed 9.2–12 GHz receiver and 9.5–14 GHz transmitter chips with 20 dB gain by using the three-dimensional (3-D) MMIC technology [2]–[14] based on a 2.5 μm × four-layer polyimide film structure. The 3-D MMIC technology effectively reduces circuit area due to its stacking effect as well as narrow line-width and spacing. The receiver integrates a four-stage front-end amplifier, an LO amplifier, and an image-rejection mixer in a 2 × 2 mm chip. The transmitter also integrates an IF amplifier with balanced outputs, an LO amplifier, an RF buffer amplifier, and a balanced upconverter in a 1.9 × 1.9 mm chip. The integration levels achieved in the X-band in receiver and transmitter are $I = 1.5$ and 2.3, respectively. These levels are nearly three times better than those previously achieved in conventional planar single-chip receivers and transmitters.

This paper describes the design method for each function block, such as low noise technique using a thin film microstrip (TFMS) line with a ground slit, higher gain matching technique using a cascode field-effect transistor (FET) with an additional connecting line, and balance compensation technique using saturated mixing FET's for an image-rejection mixer. An advanced highly integrated single-chip receiver which includes a four-stage front-end amplifier, a voltage controlled oscillator, a two-stage LO amplifier, and an image-rejection mixer is also newly demonstrated.

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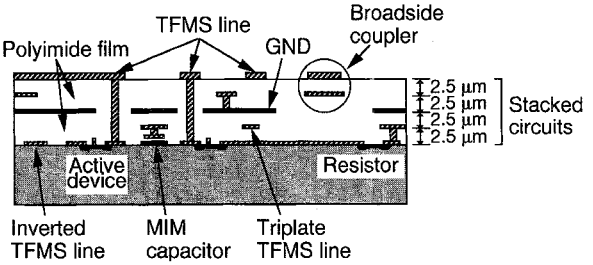


Fig. 1. Basic structure of the 3-D MMIC. Ground metal (GND) is located in the middle of the polyimide layers and passive circuits are stacked above and below the GND using narrow TFMS lines and inverted TFMS lines.

II. Three-Dimensional MMIC

Fig. 1 shows the basic structure of the 3-D MMIC. The 3-D MMIC is constructed with four layers of 2.5 μm-thick polyimide films and five layers of 1 μm-thick conductors (top conductor is 2 μm-thick) stacked on a GaAs wafer. The conductor layers are connected by through-holes to each other. Active devices, such as FET's, resistors, and MIM capacitors are formed on the substrate.

The most significant feature of the structure is that a ground metal layer is located in the middle of the polyimide layers and passive circuits are stacked above and below the ground metal. The circuits are constructed with narrow TFMS lines [3] and inverted TFMS lines with widths of 30 μm at maximum (around 10 μm on average). Another feature of the structure is a multilayer broad-side coupler which provides tight (3 dB) and wideband coupling in a small area [4]. The 3-D MMIC technology effectively reduces the circuit area and significantly increases the integration level.

III. Single-Chip Receiver Design

Fig. 2 shows a block diagram of the X-band single-chip receiver MMIC. A four-stage front-end amplifier which includes a low noise amplifier and three variable gain amplifiers, an LO amplifier, and an image-rejection mixer which includes two unit mixers, a Wilkinson divider, and a 90° hybrid are integrated in a single chip.

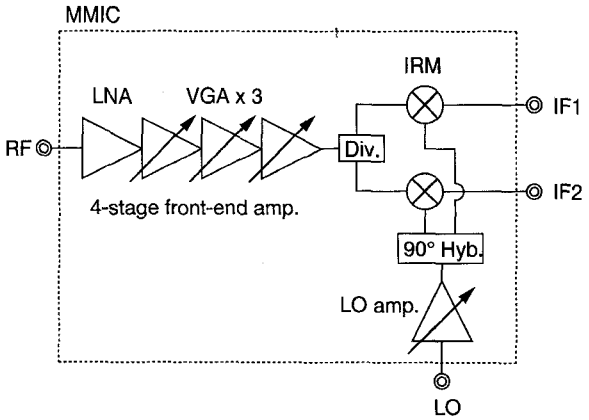


Fig. 2. Block diagram of the proposed 3-D MMIC single-chip receiver which includes a low noise amp, three variable gain amps, an LO amp, two unit mixers, a Wilkinson divider, and a 90° hybrid.

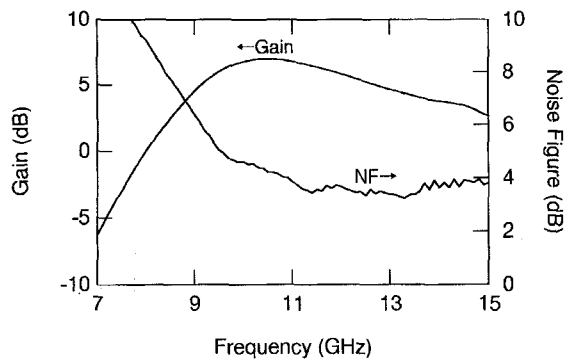


Fig. 3. Measured gain and noise figure of the fabricated 3-D MMIC low noise amplifier.

A. Low Noise Amplifier

The low noise amplifier uses a common-source-FET. A TFMS line with a ground slit below the conductor strip is employed in the input matching circuit of the low noise amplifier to increase the line-width and reduce the noise figure. This line was newly designed for the 3-D structure [12]. The characteristic impedance of 50 Ω can be obtained when both strip and slot widths are $g = 30\,\mu$m. The line is about 1.5 times wider than the conventional TFMS line (22 μm), and the loss factor is only 0.11 dB/mm at 10 GHz.

Fig. 3 shows measured gain and noise figure of the fabricated 3-D MMIC low noise amplifier. The gain and noise figure are 6.1 ± 0.9 dB and 4.2 ± 0.8 dB, respectively, from 9.2–12 GHz. The noise figure is reduced by nearly 1.5 dB from that of an amplifier with only stacked PTFMS lines for the input matching circuit.

B. Variable Gain Amplifier

Fig. 4 shows a circuit scheme of the variable gain amplifier. The variable gain amplifier employs a cascode FET which is constructed with a common-source-FET (CSF) and a common-gate-FET (CGF) connected by a nearly 3-mm-long TFMS line to achieve higher matching gain. Gain control is achieved by adjusting the second-FET gate bias voltage.

Fig. 5 shows the input- and output-impedance of the cascode FET with the line length between CSF and CGF as a parameter. By changing the line length, impedance matching can be obtained easily and insertion loss of the matching circuits can be decreased. As a result, higher matching gain can be achieved even if the line between CSF and CGF has nonnegligible loss.

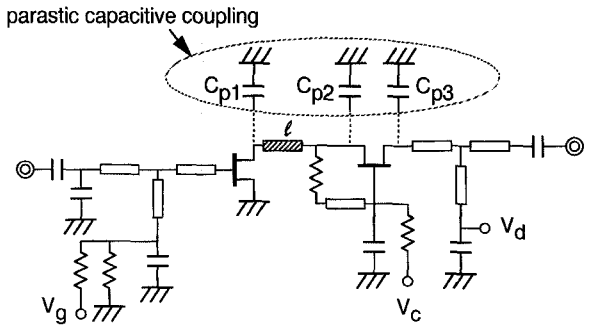


Fig. 4. Circuit scheme of the variable gain amplifier which employs a cascode FET with an additional connecting line.

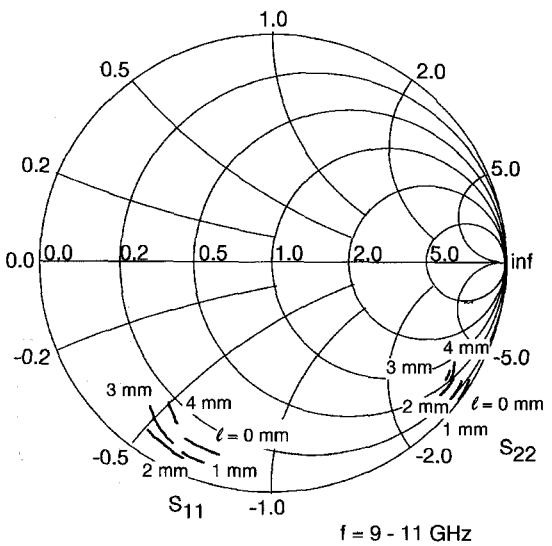


Fig. 5. Input- and output-impedance of the cascode FET with the additional connecting line length l as a parameter.

Another point to be considered in amplifier design is the capacitive coupling-effect between FET electrodes and the ground metal above the FET's. The parasitic capacitance C_ps shown in Fig. 4 are taken into account in amplifier design. The C_ps are determined by the area of the FET electrode and distance between the electrode and the ground metal just above the FET and they are around 0.02 pF in this case. The center frequency shifts to about 0.1 GHz higher when the C_ps are neglected.

Fig. 6 shows the measured gain and noise figure of the variable gain amplifier. The gain and noise figure are 8.2 ± 0.4 dB and 5.3 ± 0.3 dB, respectively, from 9.2–12 GHz. The saturation power is greater than 10 dBm. The variable gain amplifier is also used as an LO amplifier.

C. Image-Rejection Mixer

The image-rejection mixer is constructed with an RF in-phase divider, an LO 90° hybrid, and two identical unit mixers.

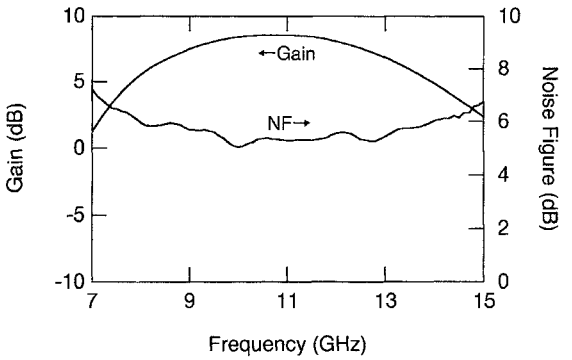


Fig. 6. Measured gain and noise figure of the fabricated 3-D MMIC variable gain amplifier.

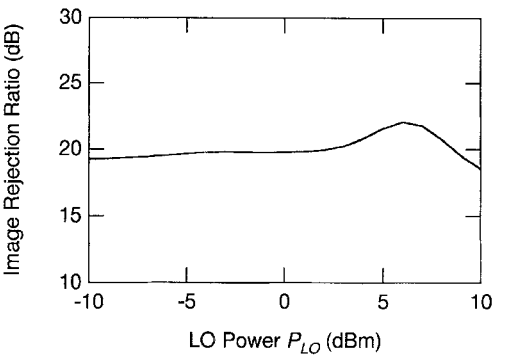


Fig. 8. Image-rejection ratio estimated from calculated amplitude and phase imbalance between two unit mixers' outputs.

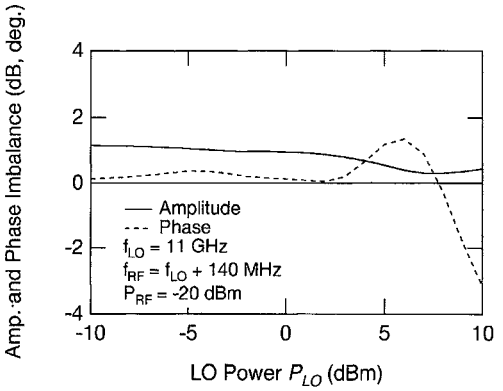


Fig. 7. Calculated amplitude and phase imbalance between two unit mixers outputs. LO input power P_{LO} and $P_{\mathrm{LO}} + 1.2$ dBm are fed to respective unit mixers.

The unit mixers employ a drain LO-injection configuration, hence no DC drain bias is required and LO-to-RF-isolation can be attained using the FET's unilateral characteristics. A multilayer broad-side coupler developed in our laboratory is used as the LO 90° hybrid to obtain a tight coupling (3 dB) in an area as small as 0.1 mm^2 [4]. The Wilkinson divider and 90° hybrid are miniaturized with meander-like TFMS lines. However, the hybrid, which is constructed with two parallel conductors located on different layers, has some imbalance in its performance because of the layer-thickness variation. To overcome this problem, we examined the condition of mixer operation and allowed for some imbalance.

The level of image rejection depends on the total amplitude and phase error of the two unit mixers' outputs which are caused by the imbalance of divider and hybrid as well as the difference between the two unit mixers. An amplitude error of less than 0.5 dB and phase error of less than 10° are required to achieve 20 dB image rejection. The measured performance of the LO 90° hybrid includes an amplitude error of 1.2 dB and phase error of 10°, and these are not enough for image-rejection mixer applications. The hybrid performance strongly depends on film thickness between the two strip conductors. The surface roughness of a multilayer dielectric film, due to variation in polyimide viscosity, may cause some deviation in the distance between the two strip conductors. This factor should be taken into account when designing the multilayer coupled-lines. The image-rejection ratio estimated from the measured performance of the hybrid is 18 dB even at the center frequency, where the two unit mixers and in-phase divider are assumed to be ideal. We employ a balance compensation technique to overcome this problem.

The key point of this technique is the use of mixing FET's saturated by the LO power. By using the saturated mixing FET's, the difference in output power becomes smaller than that of the LO input power. As a result, good amplitude and phase balance can be achieved even if the LO hybrid balance is not perfect.

Fig. 7 shows calculated amplitude and phase imbalance between two unit mixers' outputs, where LO input power P_{LO} is fed to one mixer and $P_{\mathrm{LO}} + 1.2$ dBm to the other. As the LO power increases, the amplitude balance improves. Moreover, phase error becomes large but it compensates hybrid phase imbalance. LO frequency f_{LO} is 11 GHz, RF power and frequency are -20 dBm, and $f_{\mathrm{LO}} + 140$ MHz, respectively.

Fig. 8 shows the calculated image-rejection ratio as a function of the LO input power fed to each unit mixer with 1.2 dB difference. The image-rejection ratio reaches 22 dB when total LO input power is around 10 dBm because the coupling loss of the hybrid is 4–5 dB. This result was calculated using a harmonic balance, nonlinear circuit simulator with the HP-ROOT GaAs FET model and a 200 μm-gate FET was considered. By changing the gate width of each unit mixer, we can obtain an acceptable image-rejection ratio for desired LO power. In other words, we can set the gate width to satisfy the image-rejection requirement for desired LO power. Of course, we must satisfy other design items, such as conversion loss and intermodulation characteristics.

Fig. 9 shows a measured IF output power and image rejection ratio of the fabricated image-rejection mixer as a function of LO input power. The image-rejection ratio becomes acceptable when LO input power is around 10 dBm. A 7 dB improvement of the image-rejection ratio is achieved. The balance compensation technique effectively improves the image-rejection mixer performance. RF power $P_{\mathrm{RF}} = -20$ dBm, LO frequency $f_{\mathrm{LO}} = 11$ GHz, and IF frequency $f_{\mathrm{IF}} = 140$ MHz.

IV. Single-Chip Receiver Performance

Fig. 10 shows a microphotograph of the fabricated X-band single-chip receiver. The chip size is only 2 × 2 mm. The

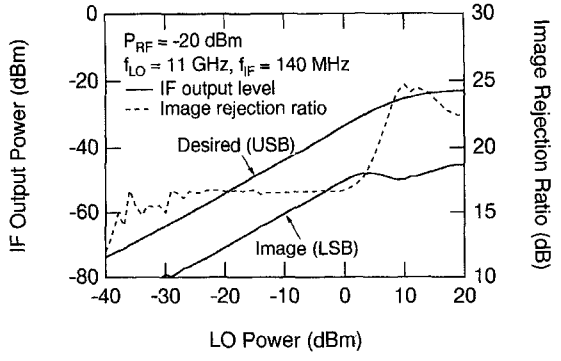


Fig. 9. Measured IF output power and image-rejection ratio of the fabricated image-rejection mixer as a function of LO input power.

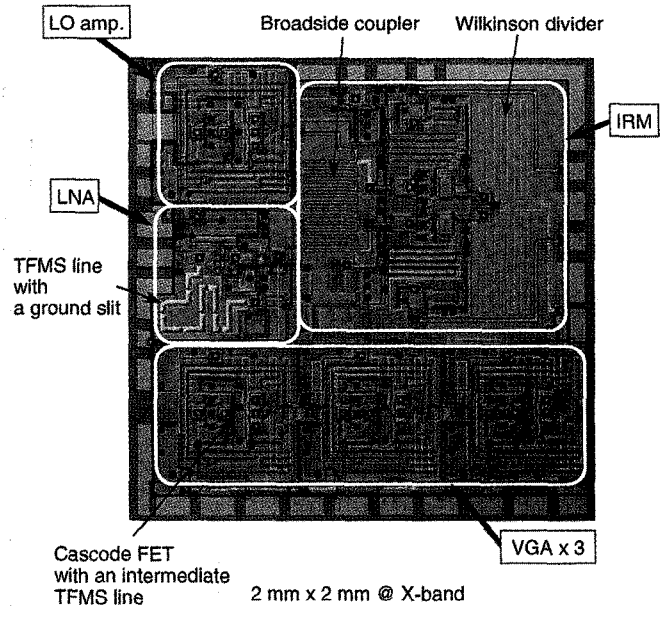


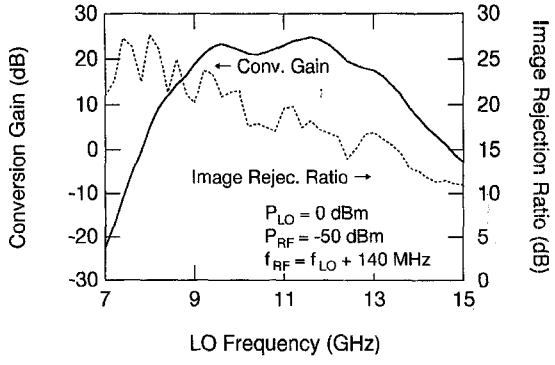
Fig. 10. Microphotograph of the fabricated X-band single-chip receiver. A low noise amp, three variable gain amp, an LO amp, and an image-rejection mixer constructed with two unit mixers, a Wilkinson divider, and a 90°C hybrid are integrated in a 2 × 2 mm chip.

layout was designed on a 3 × 3 matrix of a 0.6 × 0.6 mm spaces.

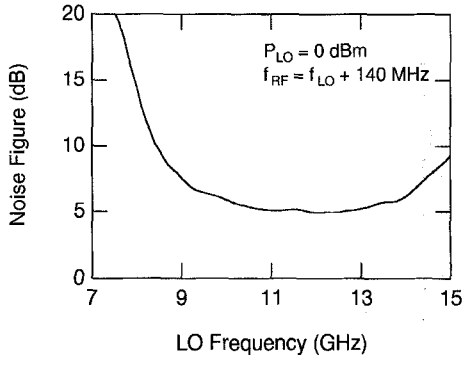
The measured performance of the single-chip receiver in the full gain condition is shown in Fig. 11. A conversion gain of 23 ± 2 dB and image-rejection ratio of better than 15 dB are obtained over the 9.2–12 GHz frequency range with a noise figure of 5.5 ± 0.5 dB, where LO power is 0 dBm, RF power is −50 dBm, and IF frequency is 140 MHz.

Fig. 12 shows the measured performance of the receiver when the conversion gain was held to −5 dB to obtain −25 dBm output power when the input power was −20 dBm. Almost the same bandwidth with flat response was obtained. The image-rejection ratio was also better than 15 dB. Gain control range was over 50 dB.

Fig. 13 shows the measured IM3 performance of the receiver as a function of RF input power per tone. The conversion gain was controlled to obtain −25 dBm output, by changing control voltages V_{c1} and V_{c2} in two different ways,



(a)



(b)

Fig. 11. Measured performance of the fabricated single-chip receiver in the full gain condition.

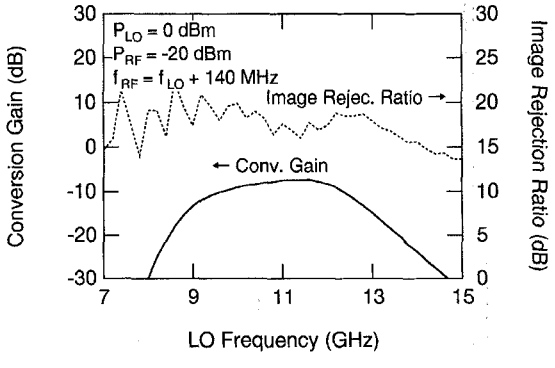


Fig. 12. Measured performance of the fabricated single-chip receiver when the gain is controlled to −5 dB to obtain −25 dBm output power when the input power is −20 dBm.

where V_{c1} and V_{c2} are the control voltages of the first and second variable gain amplifiers, respectively. In the first method, V_{c1} decreases from $V_d/2$ to $-V_d/2$ and V_{c2} holds $V_d/2$, then V_{c2} decreases from $V_d/2$ to $-V_d/2$ and V_{c1} holds $-V_d/2$ as the input power increases, where V_d is the drain bias voltage of the variable gain amplifier. In the second method, V_{c1} and V_{c2} are changed from $V_d/2$ to $-V_d/2$ simultaneously ($V_{c1} = V_{c2}$). By changing the control voltages sequentially, higher linearity can be achieved. This is because the low gain condition of the first variable gain amplifier does not significantly affect the distortion performance. LO power $P_{\mathrm{LO}} = 0$ dBm, LO frequency $f_{\mathrm{LO}} = 11$ GHz, and RF frequencies $f_{\mathrm{RF}} = f_{LO} + 140, 141$ MHz.

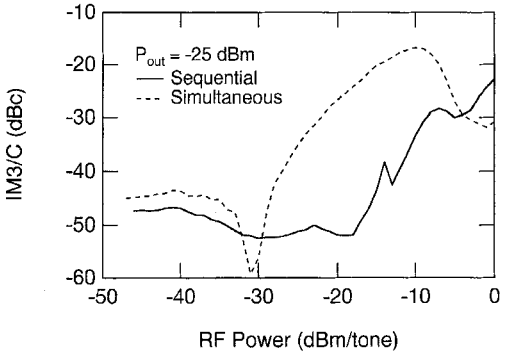


Fig. 13. Measured IM3 performance of the fabricated single-chip receiver as a function of RF input power per tone. The conversion gain is controlled to obtain −25 dBm output, where P_{LO} = 0dBm, f_{LO} = 11 GHz, and $f_{RF} = f_{LO} + 140, 141$ MHz.

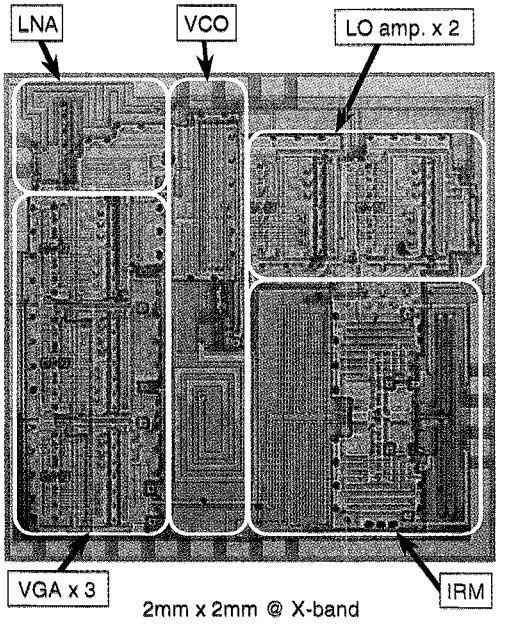


Fig. 14. Microphotograph of the advanced highly integrated 3-D MMIC single-chip receiver. The chip integrates a four-stage front-end amplifier, a voltage controlled oscillator, a two-stage LO amplifier, and an image-rejection mixer.

A. Advanced Single-Chip Receiver

Fig. 14 shows a microphotograph of a higher integrated single-chip receiver. A four-stage front-end amplifier, a voltage controlled oscillator, a two-stage LO amplifier, and an image-rejection mixer are integrated in a 2 × 2 mm chip. The amplifier and mixer configurations are almost the same as the previous one's. The voltage controlled oscillator has a conventional circuit scheme, but the resonator is constructed with a 30 μm-width TFMS line to enhance the Q factor. Higher integration has been achieved by minimizing each function block and optimizing the circuit layout. The measured conversion gain and noise figure are 24 dB and 4.9 dB in X-band, respectively.

V. Single-Chip Transmitter Design

Fig. 15 shows a block diagram of the X-band single-chip transmitter. An IF amplifier, an LO amplifier, an RF amplifier, and a balanced upconverter are integrated in a single chip. The LO and RF amplifiers are basically the same as the variable gain amplifier used in the single-chip receiver.

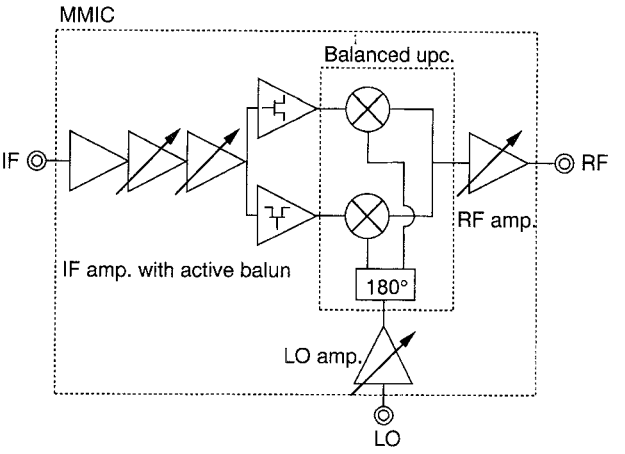


Fig. 15. Block diagram of the proposed 3-D MMIC single-chip transmitter which includes a four-stage IF amplifier with balanced outputs, an LO amp, an RF amp, two unit mixers, and an LO 180° hybrid.

A. IF Amplifier

In order to minimize the area and to achieve good balance for upconversion, the IF amplifier is an RC-coupling four-stage amplifier with balanced output ports. The first-stage of the amplifier employs a CGF to achieve active impedance matching to 50 Ω. The second and third-stages are gain control blocks using a CSF amplifier with a varistor feedback loop. The last stage of the amplifier is constructed with a combination of CGF and CSF, which is an active balun, to obtain balanced outputs.

Fig. 16 shows the measured performance of the fabricated IF amplifier. The output balance of the IF amplifier is 0.7 dB and 10° at 140 MHz. The IF amplifier is completely covered with the ground metal, so the upper portion of the IF amplifier can be used for other passive circuits.

B. Upconverter

The upconverter employs a balanced configuration. The input LO signal is divided into two signals with 180° phase difference and fed to the two unit mixers. The unit mixers for upconversion employ a gate LO-injection configuration for higher conversion gain, and both are connected at the output ports, in phase. IF signals from the IF amplifier are also fed to a gate terminal of each unit mixer. Conversion gain of 5 dB and LO suppression ratio, which is defined as the ratio of LO leak power at RF output port and LO input power, better than −20 dB are obtained.

VI. Single-Chip Transmitter Performance

Fig. 17 shows a microphotograph of the fabricated X-band single-chip transmitter. The chip size is only 1.9 × 1.9 mm. The measured conversion gain and LO suppression performance of the fabricated transmitter are shown in Fig. 18. The conversion gain and LO suppression ratio are better than 20 dB and −3

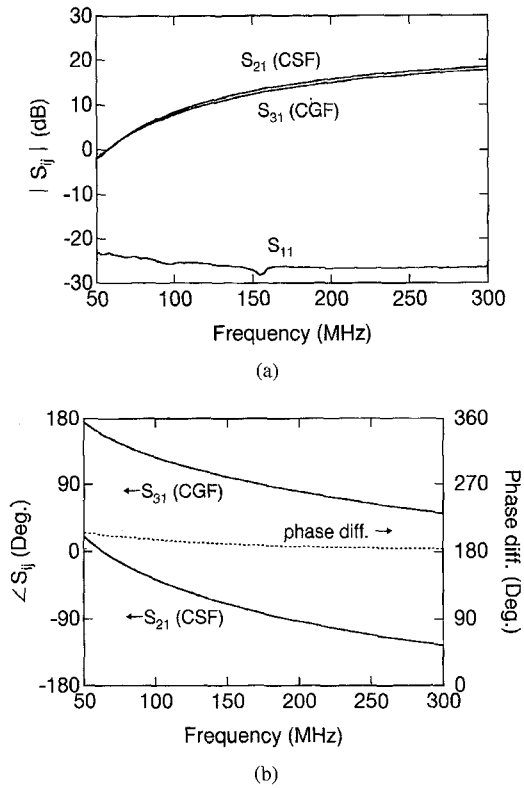


Fig. 16. Measured performance of the IF amplifier.

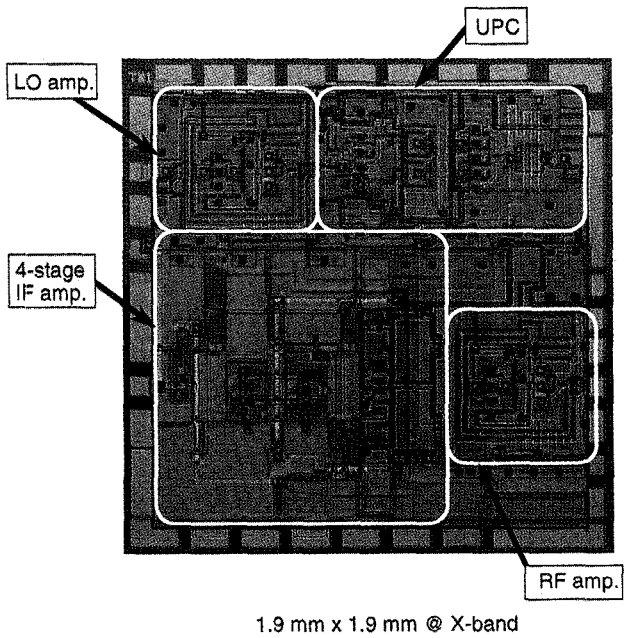


Fig. 17. Microphotograph of the fabricated X-band single-chip transmitter. A four-stage IF amplifier with an active balun, an LO amp, an RF amp, and a balanced upconverter are integrated in a 1.9 × 1.9 mm chip.

dB over the very wideband range of 9.5–14 GHz, respectively. LO power is 0 dBm, IF frequency and power are 140 MHz and −20 dBm, respectively.

Fig. 19 shows the measured IM3 performance of the transmitter. D/U is better than 50 dB when RF output power is −10 dBm. A third-order intercept point (IP3) of 15 dBm is

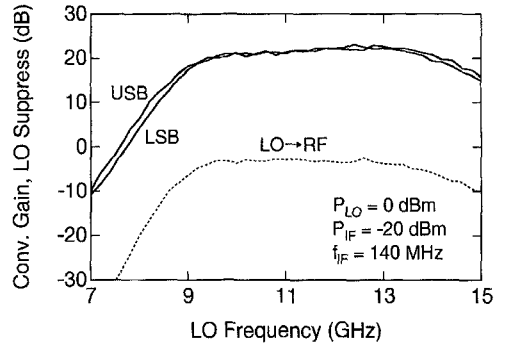


Fig. 18. Measured conversion gain and LO suppression ratio of the fabricated 3-D MMIC single-chip transmitter.

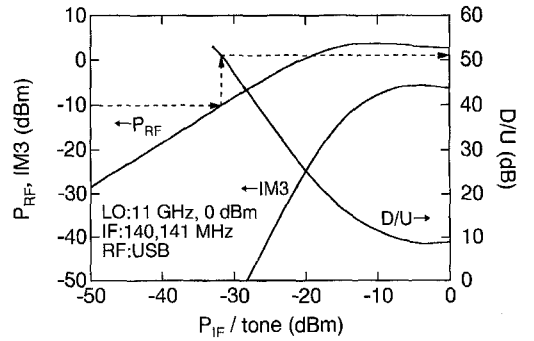


Fig. 19. Measured IM3 performance of the single-chip transmitter. D/U of better than 50 dB is obtained when RF output power is −10 dBm.

achieved. LO power is 0 dBm, LO frequency is 11 GHz, and IF frequencies are 140 and 141 MHz.

VII. Conclusion

Single-chip X-band receiver and transmitter MMIC's which effectively use the 3-D MMIC technology have been demonstrated. Integration levels have been significantly increased to nearly three times that obtained heretofore. The 3-D MMIC is a promising technology in the development of highly integrated multifunctional MMIC's, and can be effectively applied for many kinds of wireless communication systems.

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